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## Complete if Known

Application Number	09/542,024
Filing Date	April 3, 2000
First Named Inventor	BERGAMASCHI
Group Art Unit	2123
Examiner Name	Unassigned
Attorney Docket Number	YOR-2000-0054

## OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
NL	A	"VSI Alliance Architecture Document", Version 1.0, VSI Alliance, 1997.	
NL	B	A.M. RINCON et al., "The Changing Landscape of System-on-a-Chip Design", IBM MicroNews, Vol.5, No. 3, pp. 1-9, IBM Microelectronics, 3rd Quarter, 1999.	
NL	C	"The CoreConnect Bus Architecture", IBM Corporation, pp. 1-8, 1999.	
NL	D	A.M. RINCON et al., "Core Design and System-on-a-Chip Integration", IEEE Design & Test of Computers, pp. 26-35, October/December, 1997.	
NL	E	P. SCHINDLER et al., "IP Repository, A Web based IP Reuse Infrastructure", IEEE Custom Integrated Circuits Conference, pp. 415-418, May, 1999.	
NL	F	R.E. BRYANT, "Graph-Based Algorithms for Boolean Function Manipulation", IEEE Transactions on Computers, Vol. C-35, No. 8, August 1986, pp. 677-691.	
NL	G	W.P. BIRMINGHAM et al., "MICON: Automated Design of Computer Systems", Engineering Design Research Center, Carnegie Mellon University, Pittsburgh, PA.	

Examiner Signature

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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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